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10/699,939

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(836)

4358

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03/09/2005

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EXAMINER

TRIEU, VAN THANH

ART UNIT

PAPER NUMBER

2636

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/699,939

Applicant(s)

FISLER ET AL.

Examiner

Van T Trieu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 and 25 is/are rejected.
- 7) ☒ Claim(s) 24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/03/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## ***DETAILED ACTION***

### ***Drawings***

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawing papers are draft paper having lines. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

### ***Claim Objections***

2. Claim 1 is objected to because of the following informalities: line 6, there is a quote "" between the phrase "operation'responsive". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by **Deutsch et al** [US 4,932,246].

Regarding claim 1, the claimed alarm indicating apparatus comprising: a source of first synchronizing control pulses usable to synchronize alarm indicating output devices in a first, normal, mode of operation (the controller 11 generates a first primary modulation PM comprising pulse width to the driver stages 12 and associated loads 13 for determining the driver stage 12 on/off operation status for a first time period T, see Figs. 1, 4 and 5, col. 2, lines 34-43, col. 4, lines 53-68 and col. 5, lines 1-2); and the at least one output device coupled to the source, via the communication medium, the device having a normal mode of operation responsive to the first control pulses and a second mode of operation, activated for a limited, predetermined time interval, upon being coupled to the medium, and responsive to different control pulses whereupon the output device emits at least one non-alarm indicium indicative of normal device operation, which reads upon the controller 11 also generates a test mode with a second sub-modulation signal SM of high frequency pulses for testing exit continuously between the first predetermined time period T for proper operation and developing a fault signal in response to improper operation. The fault flag register processes to provide a warning to the vehicle operator the precise nature of the detected fault and which driver stages 12 the fault was detected in, wherein the warning/indicating is connected to the fault flag register and the controller 11, or the operator can verify in both on and off states of the device if its operation is proper, see Figs. 1-5, col. 2, lines 43-56, col. 3, lines 4-59, col. 5, lines 2-68, col. 6, lines 1-68, col. 7, lines 1-19, col. 13, lines 37-68 and col. 14, lines 1-21.

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Regarding claim 2, all the claimed subject matters are cited in respect to claim 1 above, and including the circuitry to switch to a normal mode of operation in the absence of the different set of control pulses (the control circuit has applicability to on/off driver stages 12 use for controlling other loads operating normally, wherein each driver stages 12 has different set of modulation pulses and sub-modulation pulses, see Figs. 1 and 5.

Regarding claim 3, all the claimed subject matters are cited in respect to claim 2 above.

Regarding claim 4, all the claimed subject matters are cited in respect to claim 1 above, and including the program processor (the microprocessor controller 11 is a computer programmable, see Fig. 6, col. 4, lines 35-67, col. 5, lines 1-68 and col. 6, lines 1-38).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

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not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 5-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Deutsch** [US 4,932,246].

Regarding claim 5, **Deutsch et al** fails to disclose the additional plurality of output devices coupled to the medium, the plurality of output devices responds to the different set of control pulses and does not enter the normal mode operation. However, **Deutsch et al** teaches that the microprocessor controller 11 is programmed to generates different set of sub-modulation pulses in test mode for each driver stages 12 and loads 13, and different addresses according thereto, so that the controllers 11 can identify and indicating exactly of the fault detected to the vehicle operator, see Figs. 1, 5 and 6, col. 11, lines 3-41, col. 13, lines 37-68 and col. 14, lines 1-21. Since the conventional vehicle has built with a plurality of alarming/warning outputs such as horn, speakers, tone, LED light and/or LCD display to assure that the operator/driver notice of the alarming/warning messages. Therefore, it would have been obvious to one skill in the art at the time the invention was made to implement the driver stages and loads operation status to both the audio and visual alarming/warning output devices built with the vehicle for higher recognized of the status by the driver/operator.

Regarding claim 6, all the claimed subject matters are discussed in respect to claim 5 above, see Figs. 5C-5F.

Regarding claim 7, all the claimed subject matters are discussed in respect to claim 6 above, see Fig. 1.

Regarding claim 8, all the claimed subject matters are discussed in respect to claims 1 and 5 above.

Regarding claim 9, all the claimed subject matters are discussed in respect to claim 8 above, and the non-alarm audio output or a non-alarm visual output, which reads upon the fault signals to shut down the driver stage and/or to prevent further testing that fault stage, see col. 14, lines 1-10.

Regarding claim 10, all the claimed subject matters are discussed in respect to claims 1 and 5 above, and the transducer, which reads upon the audio output devices such as piezoelectric, transducer and/or speaker to generate sound alarm.

Regarding claim 11, all the claimed subject matters are discussed in respect to claims 1 and 10 above.

Regarding claim 12, all the claimed subject matters are discussed in respect to claims 4 and 10 above.

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Regarding claim 13, all the claimed subject matters are discussed in respect to claims 1 and 12 above.

Regarding claim 14, all the claimed subject matters are discussed in respect to claims 8 and 10 above.

Regarding claim 15, all the claimed subject matters are discussed in respect to claims 4 and 14 above.

Regarding claim 16, all the claimed subject matters are discussed in respect to claims 1 and 15 above.

Regarding claim 16 the claimed port for receipt of electrical and control signal (the outputs of primary modulation PM cables and sub-modulation SM cables to each of the driver stages 12 and loads 13, see Fig. 1); but **Deutsch et al** fails to disclose the control circuitry, coupled to the port for receipt of the control signals, including circuitry for responding to the control signals to enter at least an install output mode, the install output mode being entered into in the on-going presence of the install mode control signals. However, **Deutsch et al** teaches that the microprocessor controller 11 has a plurality of ports for transmitting the control signals to each of the driver stages 12 with associated load 13 with a sub-modulation SM in diagnostic fault test mode. In response to the SM signal, the controller 11 provides an output signal indicating whether or not



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the driver stage 12 being normal operation, see Figs. 1-6, col. 2, lines 34-68 and col. 3, lines 1-44. Therefore, it would have been obvious to one skill in the art to recognize that the diagnostic fault test mode is functionally equivalent to the claim install output mode because most of the electronic and electrical equipment and/or system being tested for all of the operational functions after installed to assure of the quality products and to prevent of any malfunction to cause accident or damage to the system.

Regarding claim 18, all the claimed subject matters are discussed in respect to claim 17 above, and the processor and instructions executable (the programmable microprocessor 11 executes the test or install mode, see Figs. 1 and 6).

Regarding claim 19, all the claimed subject matters are discussed in respect to claims 1 and 17 above.

Regarding claim 20, all the claimed subject matters are discussed in respect to claims 1, 8 and 17 above.

Regarding claim 21, the method claimed limitations are met by the apparatus discussed in respect to claims 1 and 8 above.

Regarding claim 22, all the claimed subject matters are discussed in respect to claims 1 and 21 above.

Regarding claim 23, all the claimed subject matters are discussed in respect to claims 13 and 21 above.

Regarding claim 25, all the claimed subject matters are discussed in respect to claims 8 and 21 above, see Fig. 1.

### ***Conclusion***

5. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Tanizaki et al** discloses a control circuit generating various commands for a memory cell array according to an internal command control signal and internal address signal output from an input switching circuit for switching an input source of the command control signals and the address signal between an external terminal and a built in self test BIST circuit when the semiconductor memory device is installed on a circuit board.


[US 6,782,498]

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**Lowry, Sr.** discloses an apparatus and method for detecting overstroke, understroke an/or overspeed, underspeed condition in vibratory equipment. A control circuit means is operable by an abnormal pulse to generate an alarm and/or shut down the vibrating equipment. [US 4,369,398]

7. Any inquiry concerning this communication or earlier communications from examiner should be directed to primary examiner **Van Trieu** whose telephone number is (571) 272-2972. The examiner can normally be reached on Mon-Fri from 7:00 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. **Jeffery Hofsass** can be reached on (571) 272-2981.



**Van Trieu**  
**Primary Examiner**  
**Date: 3/4/05**